RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2628

PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Dong-Woo LEE and Ja-Il KOO		
Serial No.:	09/898,699	Examiner:	Singh, Dalip K.
Filed:	July 2, 2001	Group Art Unit:	2671
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For:	MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE		

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Advisory Action, Paper No. 51906, dated March 31, 2006, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

IN THE CLAIMS

1. (Currently amended) A memory device for use with a memory controller, the memory device comprising:

a memory cell array adapted to store internal depth data of an object;

a compare circuit;

a line connecting the compare circuit to the memory cell array; and

a data modifying circuit distinct from the memory controller, the data modifying circuit including the compare circuit and being adapted to:

receive corresponding new external depth data of the object from the memory controller,

compare the new external depth data with the internal depth data, ~~and~~

transfer ~~write~~ the external depth data, via the connecting line, into the memory cell array, depending on the result of the comparison,

if the external depth data is transferred, over-write the internal depth data with the transferred external depth data ~~depending on the result of the comparison~~, and

output to the memory controller a status signal.

2. (Cancelled)

3. (Original) The memory device of claim 1, further comprising:

a first control pin for receiving a first control signal from the memory controller; and

a control circuit for transmitting the external depth data to the memory cell array thereby bypassing the data modifying circuit depending on a state of the first control signal.

4. (Cancelled)

5. (Currently amended) The memory device of claim 3[[4]], wherein the status signal is output through the first control pin.

6. (Previously presented) The memory device of claim 1, wherein the data modifying circuit includes

a register for storing the received new external depth data, wherein the compare circuit is adapted to compare the stored new external depth data with the internal depth data, and adapted to write the external depth data, via the connecting line, into the memory cell array depending on the result of the comparison.

7. (Original) The memory device of claim 6, wherein the compare circuit is further adapted to write the external depth data in the memory cell array if the external depth data is smaller than the internal depth data.

8. (Original) The memory device of claim 6, wherein the compare circuit is further adapted to output a status signal to the memory controller.

9. (Original) The memory device of claim 6, further comprising:

a second control pin for receiving a second control signal from the memory controller,

wherein the compare circuit compares the internal depth data with the stored external depth data in units of X bits when the second control signal is in a non-active state, and in units of NX bits when the second control signal is in an active state.

10. (Original) The memory device of claim 9, wherein

if the second control pin is in an inactive state, the compare circuit outputs to the memory controller:

a first status signal indicating that the lower X bits of the internal depth data have been modified, and

a second status signal indicating that the upper X bits of the internal depth data have been modified.

11. (Original) The memory device of claim 9, wherein

if the second control pin is in a non-active state, the compare circuit outputs to the memory controller a status signal indicating that NX bits of the internal depth data have been modified.

12. (Currently amended) A method of processing depth data of an object in a memory device controlled by a memory controller, the method comprising:

receiving external depth data of the object from the memory controller;

storing the received external depth data;

receiving a first control signal from the memory controller through a first control pin distinct from the memory controller;

determining a state of the first control signal;

if the state of the first control signal is determined to be inactive, writing the external depth data to a memory cell array within the memory device,

else if the state of the first control signal is determined to be active,

receiving the stored external depth data and corresponding internal depth data stored in the memory cell array at a compare circuit that is distinct from the memory controller and connected via a line to the memory cell array, comparing[[,]] the received data,

writing from the compare circuit~~, via the connected line,~~ the external depth data over the corresponding internal depth data in[[to]] the memory cell array by transferring the external depth data via the connected line, depending on the result of the comparison, and

outputting to the memory controller a status signal indicating that the internal depth data has been modified;

receiving a second control signal from the memory controller through a second control pin distinct from the memory controller;

determining a state of the second control signal; and

if the state of the second control signal is determined to be inactive, comparing the internal depth data with the stored external depth data in units of X bits,

elseif the state of the second control signal is determined to be active, comparing the internal depth data with the stored external depth data in units of NX bits,

wherein comparing the internal depth data with the stored external depth data in units of NX bits further includes

outputting to the memory controller a status signal indicating that the NX bits of the internal depth data has been modified.

13. (Cancelled)

14. (Previously presented) The method of claim 12, wherein

writing the external depth data takes place if the comparison yields that the external depth data is smaller than the internal depth data.

15. (Previously presented) The method of claim 12, wherein

writing the external depth data takes place if the comparison yields that the external depth data is larger than the internal depth data.

16. (Cancelled)

17. (Previously presented) The method of claim 12, wherein comparing the internal depth data with the stored external depth data in units of X bits further includes

outputting to the memory controller a first status signal indicating that the lower X bits of the internal depth data have been modified, and

outputting to the memory controller a second status signal indicating that the upper X bits of the internal depth data have been modified.

18. (Original) The method of claim 17, wherein the first status signal is output through the first control pin, and the second status signal is output through the second control pin.

19. (Cancelled)

20. (Previously presented) The method of claim 12, wherein the status signal is output through one of the first and second control pins.

21-23. (Cancelled)

24. (Previously presented) The memory device of claim 1, further comprising a first control pin that directly connects the compare circuit to the memory controller.

25. (Previously presented) The memory device of claim 24, wherein the first control pin is adapted to receive a first control signal from the memory controller and to output a first status signal to the memory controller.

26. (Previously presented) The memory device of claim 25, further comprising a second control pin that directly connects the compare circuit to the memory controller.

27. (Previously presented) The memory device of claim 26, wherein the second control pin is adapted to receive a second control signal from the memory controller and to output a second status signal to the memory controller.

28. (New) A memory device for use with a memory controller, the memory device comprising:

a memory cell array adapted to store internal depth data of an object;

a compare circuit;

a line connecting the compare circuit to the memory cell array; and

a data modifying circuit distinct from the memory controller, the data modifying circuit including the compare circuit and being adapted to:

receive corresponding new external depth data of the object from the memory controller via a control circuit that is responsive to a control signal directly from the compare circuit,

compare the new external depth data with the internal depth data,

transfer the external depth data, via the connecting line, into the memory cell array, depending on the result of the comparison,

if the external depth data is transferred, over-write the internal depth data with the transferred external depth data, and

output to the memory controller a status signal.

29. (New) The memory device of claim 28, wherein the control circuit is adapted to transmit the external depth data to the memory cell array thereby bypassing the data modifying circuit, depending on a state of the control signal.

30. (New) The memory device of claim 29, wherein the data modifying circuit includes a register for storing the received new external depth data, wherein the compare circuit is adapted to compare the stored new external depth data with the internal depth data, and adapted to write the external depth data by transferring the external depth data via the connecting line into the memory cell array depending on the result of the comparison.

31. (New) The memory device of claim 30, wherein the compare circuit is further adapted to write the external depth data in the memory cell array if the external depth data is smaller than the internal depth data.

REMARKS

Claims 1, 3, 5-12, 14, 15, 17, 18, 20 and 24-27 are pending.

Claims 1 and 24-27 were rejected under 35 U.S.C. 102(b).

Claims 3-15, 17, 18 and 20 were rejected under 35 U.S.C. 103(a).

Claims 2, 4, 13, 16, 19 and 21-23 are cancelled without prejudice.

No new matter is added.

Applicant request reconsideration and allowance of the claims in view of the remarks below.

Interview Summary

Applicant thanks the Examiner for the brief telephone discussion that was conducted between the Examiner and Applicant's representative, Brian Wichner, on August 22, 2006. During that discussion, Applicant's representative pointed out that writing new external depth data via a connecting line, as in claims 1 and 12, is different than sending a write enable signal over a connecting line, which is all that Deering teaches. In any case, the Examiner acknowledged that amending the claims with an added limitation that more directly describes the external depth data itself being transferred via the connecting line will overcome the rejections in view of Deering.

Claim Objections

Applicant has cancelled claim 4. Claim 5 has been amended to depend upon claim 3.

Claim Rejections – 35 U.S.C. § 102

Claims 1 and 24-27 were rejected under 35 U.S.C. 102(b) as being anticipated by Deering U.S. Patent 5,544,306 ("Deering").

Claim Rejections – 35 U.S.C. § 103

Claims 3-15, 17, 18 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Deering in view of Dowdell U.S. Patent No. 5,301,263 ("Dowdell").

Applicant respectfully traverses the rejection.

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As mentioned in the Interview Summary above, applicants maintain that writing new external depth data via a connecting line, as in claims 1 and 12, is different than sending a write enable signal over a connecting line, which is all that Deering teaches. Even so, in order to advance the case towards allowance, applicant amends the claims with the added limitation that *the external depth data is transferred, via the connecting line, into the memory cell array, depending on the result of the comparison, and if the external depth data is transferred, over-write the internal depth data with the transferred external depth data.*

New Claims

Claims 28-31 are new and novel in view of Deering and Dowdell, individually or in combination. No new matter has been added. For example, claim 28 recites a data modifying circuit adapted to receive corresponding new external depth data of the object from the memory controller via a control circuit that is responsive to a control signal directly from the compare circuit. Neither of the cited references teaches this or other limitations of the new claims.

Conclusion

For the foregoing reasons, reconsideration and allowance of the claims of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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